FIG.1

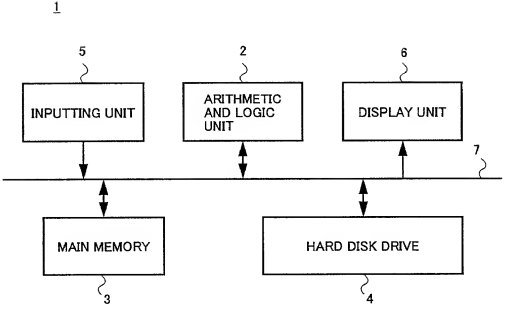
1
5
2
6
INPUTTING UNIT
ARITHMETIC AND LOGIC UNIT
DISPLAY UNIT
7
MAIN MEMORY
HARD DISK DRIVE
3
4

FIG.2

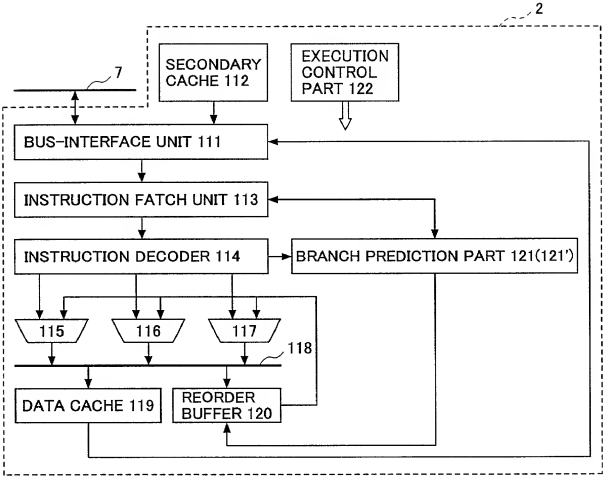
2
7
SECONDARY CACHE 112
EXECUTION CONTROL PART 122
BUS-INTERFACE UNIT 111
INSTRUCTION FATCH UNIT 113
INSTRUCTION DECODER 114
BRANCH PREDICTION PART 121(121')
115
116
117
118
DATA CACHE 119
REORDER BUFFER 120

FIG. 3

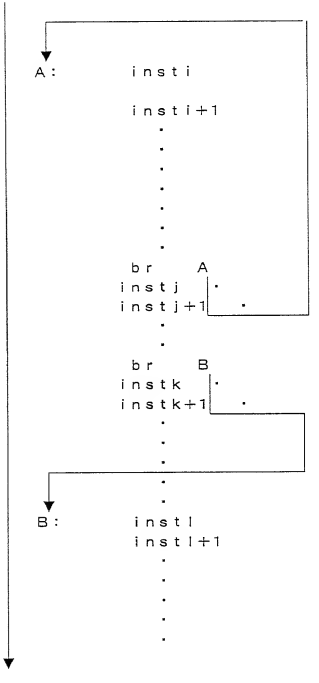
A:
insti
insti+1
br A
instj
instj+1
br B
instk
instk+1
B:
instl
instl+1

FIG.4

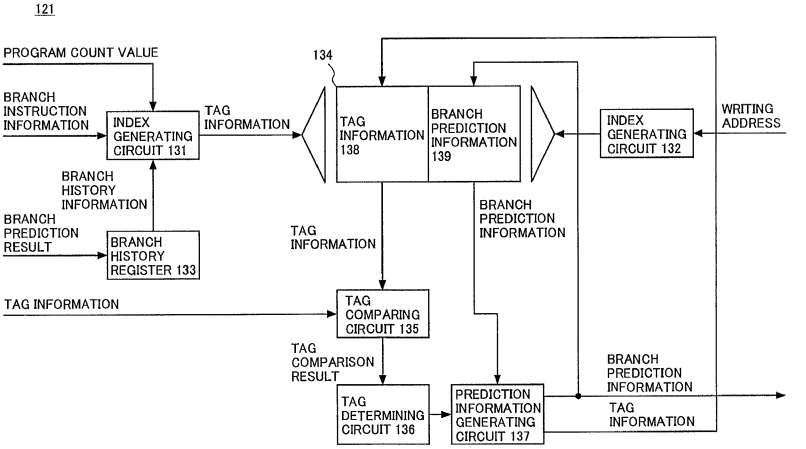
121
PROGRAM COUNT VALUE
134
BRANCH INSTRUCTION INFORMATION
INDEX GENERATING CIRCUIT 131
TAG INFORMATION
TAG INFORMATION 138
BRANCH PREDICTION INFORMATION 139
INDEX GENERATING CIRCUIT 132
WRITING ADDRESS
BRANCH HISTORY INFORMATION
BRANCH PREDICTION RESULT
BRANCH HISTORY REGISTER 133
TAG INFORMATION
BRANCH PREDICTION INFORMATION
TAG INFORMATION
TAG COMPARING CIRCUIT 135
TAG COMPARISON RESULT
BRANCH PREDICTION INFORMATION
TAG DETERMINING CIRCUIT 136
PREDICTION INFORMATION GENERATING CIRCUIT 137
TAG INFORMATION

FIG. 5

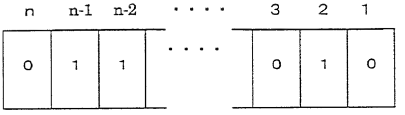

FIG. 6

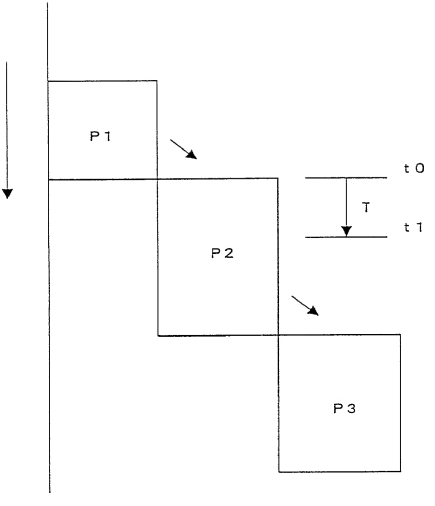

FIG.7

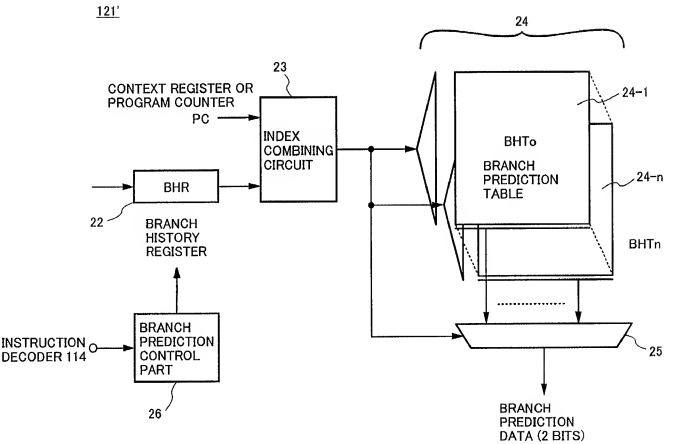
121'
24
23
CONTEXT REGISTER OR
PROGRAM COUNTER
PC
INDEX
COMBINING
CIRCUIT
24-1
BHTo
BRANCH
PREDICTION
TABLE
24-n
BHTn
BHR
22
BRANCH
HISTORY
REGISTER
INSTRUCTION
DECODER 114
BRANCH
PREDICTION
CONTROL
PART
26
25
BRANCH
PREDICTION
DATA (2 BITS)

FIG.8

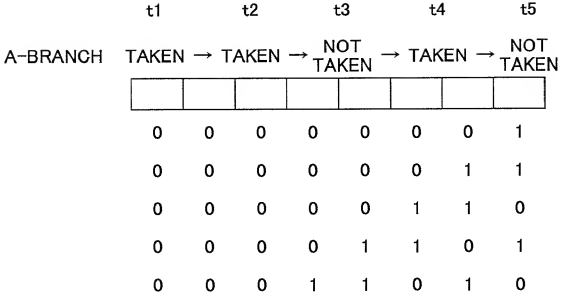
t1
t2
t3
t4
t5
A-BRANCH
TAKEN → TAKEN → NOT TAKEN → TAKEN → NOT TAKEN
0 0 0 0 0 0 0 1
0 0 0 0 0 0 1 1
0 0 0 0 0 1 1 0
0 0 0 0 1 1 0 1
0 0 0 1 1 0 1 0

FIG. 9

a	b	c
ax	b1	01
ax	b2	00
ax	b3	
⋮	⋮	⋮
ax	bm	11

25－X

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FIG. 10

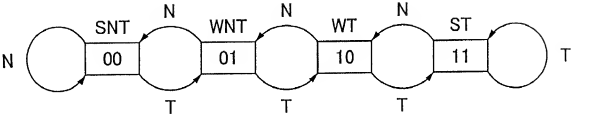

FIG.11

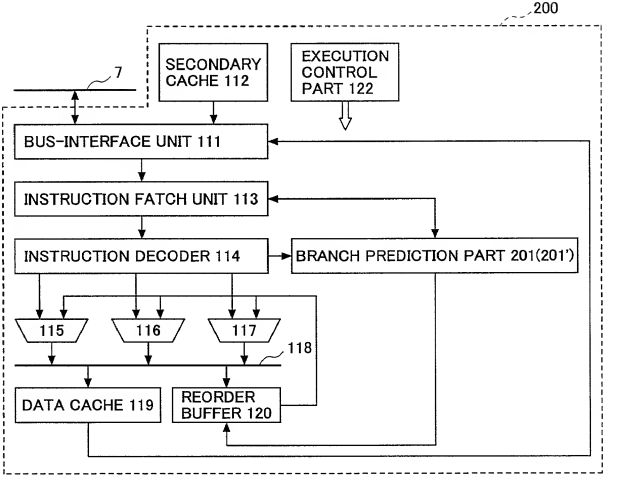
200
7
SECONDARY CACHE 112
EXECUTION CONTROL PART 122
BUS-INTERFACE UNIT 111
INSTRUCTION FATCH UNIT 113
INSTRUCTION DECODER 114
BRANCH PREDICTION PART 201(201')
115
116
117
118
DATA CACHE 119
REORDER BUFFER 120

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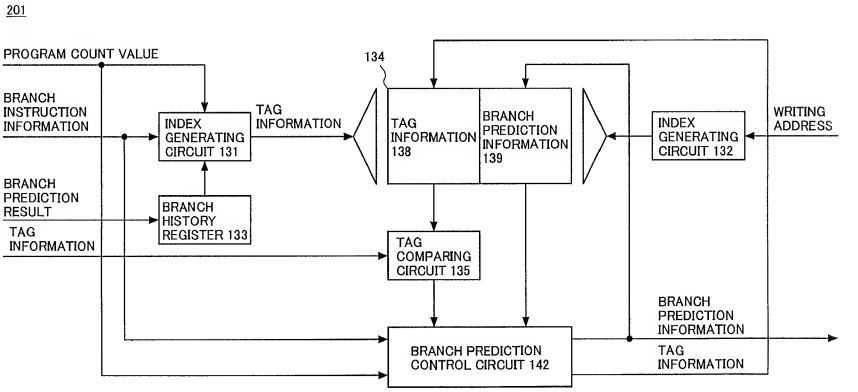
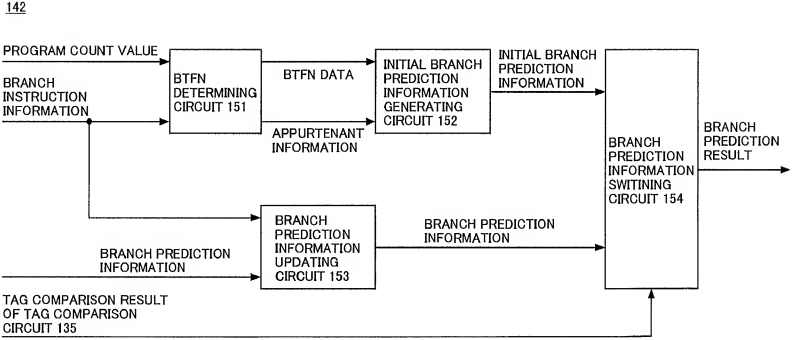
FIG.12



0051 2T*ES1 9E760

FIG.13



00512T"ES19C760

FIG.14

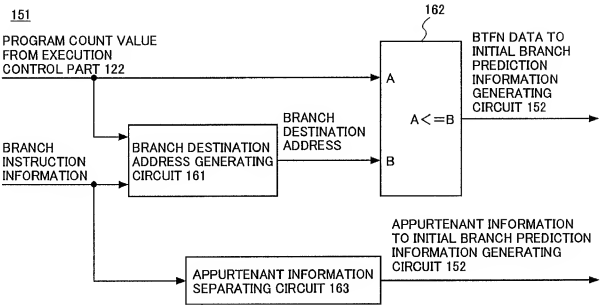


FIG.15

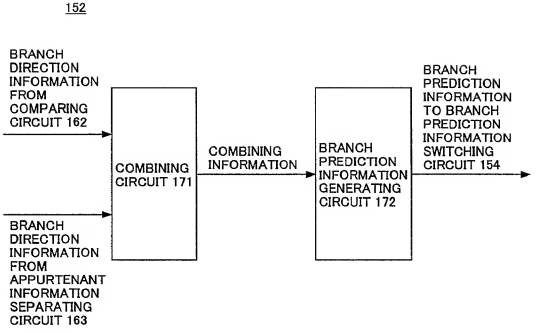
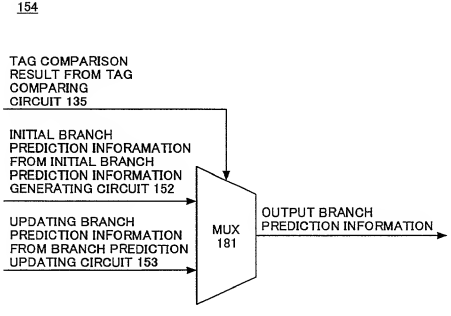

152
BRANCH DIRECTION INFORMATION FROM COMPARING CIRCUIT 162
BRANCH DIRECTION INFORMATION FROM APPURTENANT INFORMATION SEPARATING CIRCUIT 163
COMBINING CIRCUIT 171
COMBINING INFORMATION
BRANCH PREDICTION INFORMATION GENERATING CIRCUIT 172
BRANCH PREDICTION INFORMATION TO BRANCH PREDICTION INFORMATION SWITCHING CIRCUIT 154

FIG.16


154
TAG COMPARISON RESULT FROM TAG COMPARING CIRCUIT 135
INITIAL BRANCH PREDICTION INFORAMATION FROM INITIAL BRANCH PREDICTION INFORMATION GENERATING CIRCUIT 152
UPDATING BRANCH PREDICTION INFORMATION FROM BRANCH PREDICTION UPDATING CIRCUIT 153
MUX 181
OUTPUT BRANCH PREDICTION INFORMATION

00512T'E9T9E760

FIG.17

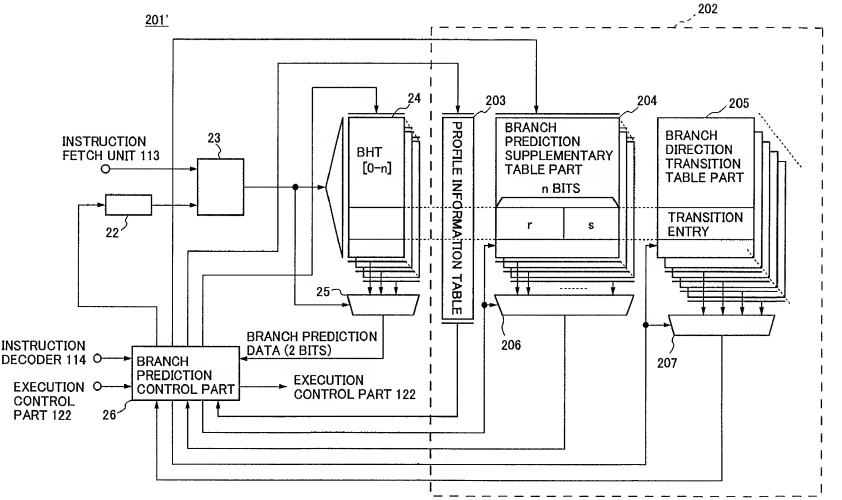


FIG.18

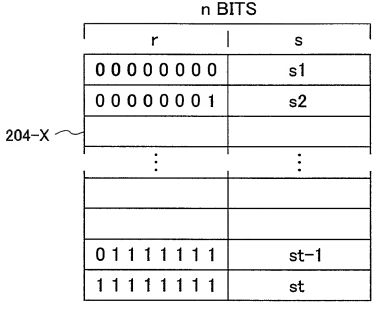

n BITS
r
s
000000000
s1
000000001
s2
204-X
01111111
st-1
11111111
st

FIG.19

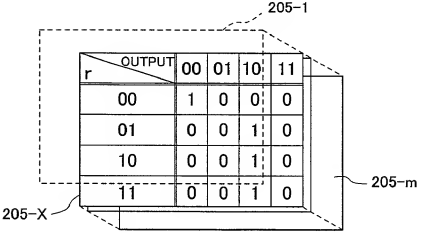
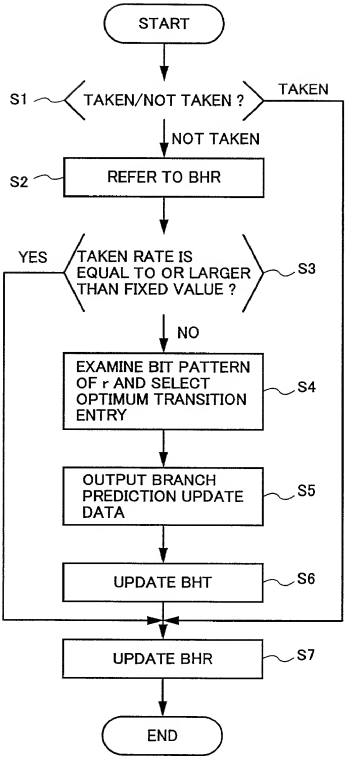

205-1
r
OUTPUT
00
01
10
11
00
1
0
0
0
01
0
0
1
0
10
0
0
1
0
11
0
0
1
0
205-X
205-m

FIG.20


START
S1
TAKEN/NOT TAKEN ?
TAKEN
NOT TAKEN
S2
REFER TO BHR
YES
TAKEN RATE IS EQUAL TO OR LARGER THAN FIXED VALUE ?
S3
NO
EXAMINE BIT PATTERN OF r AND SELECT OPTIMUM TRANSITION ENTRY
S4
OUTPUT BRANCH PREDICTION UPDATE DATA
S5
UPDATE BHT
S6
UPDATE BHR
S7
END

0057287 EP 2 375 760

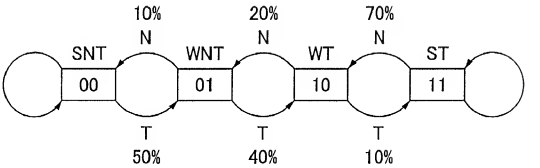



FIG. 21